Note Title 4/13/2009

Take-home Test 2 due Friday, April 17

Latches and flip-flops (Ch 11)

Sequential circuits are circuits with memory, i.e., the output of a sequential circuit depends not only on the current inputs but also on the sequence of previous inputs.

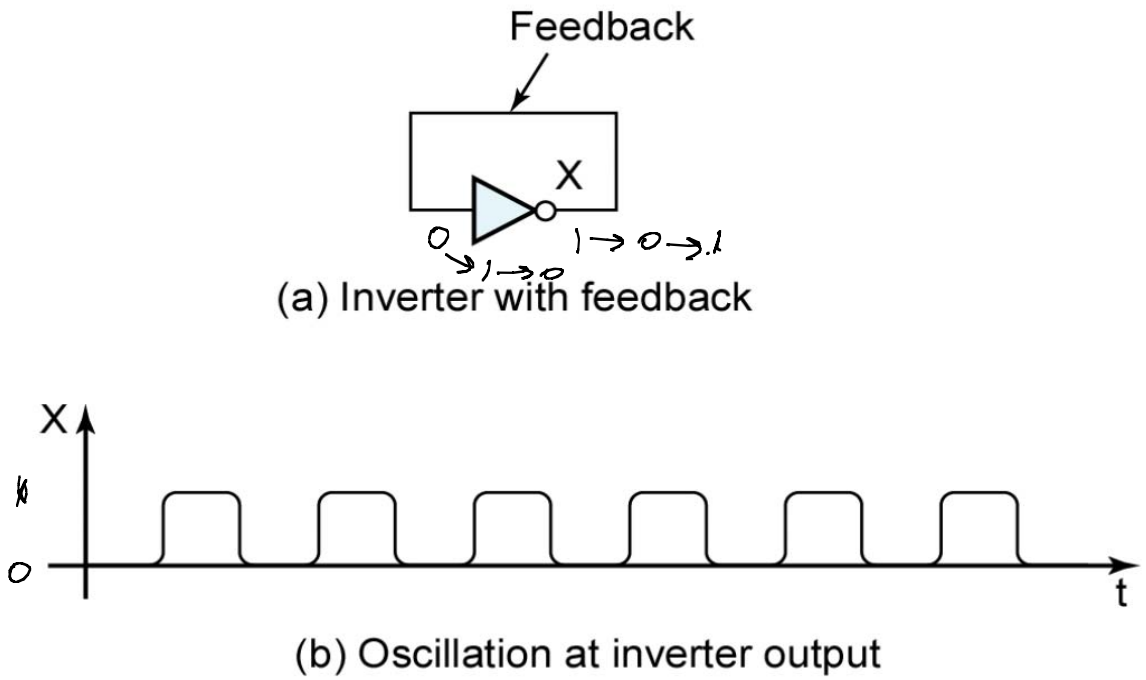
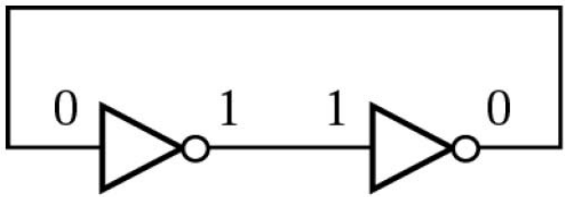


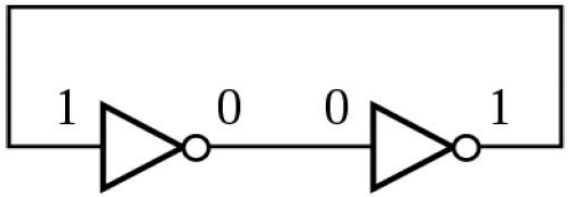
Figure 11-1

To get memory, we use feedback.

In this circuit, feedback is used, but there is no memory!



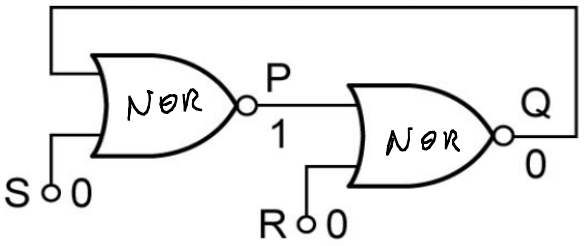
(a)



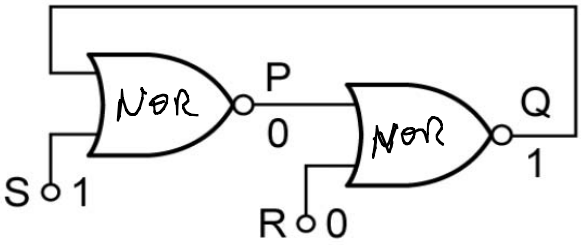
(b)

Figure 11-2

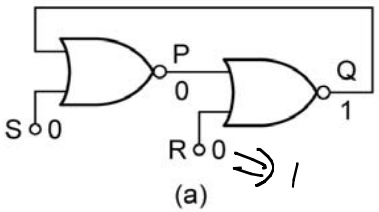
This circuit (with feedback) has two stable states.
(a) and (b)



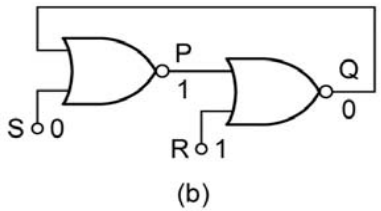
(a)



(b)



(a)



(b)

Figure 11-4

In a latch, there is no seperate clock input; in a flip-flop, there is.

(a) is a stable configuration

In (b), we take (a) and change S to 1. The circuit moves to the new configuration displayed in (b). This configuration (is stable.)

Change S back to 0. Surprise! P and Q remain the same, and 11-4(a) is stable!

Change R to 1, Q changes to 0 and P changes to 1, and 11-4(b) is stable.

R = S = 1 is not allowed.

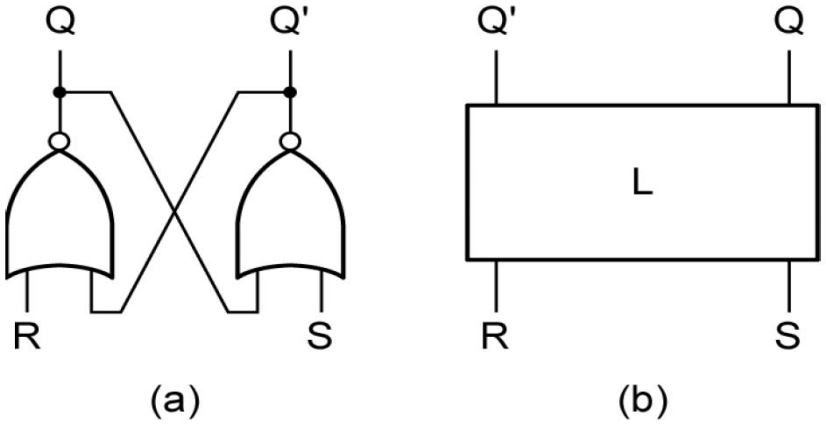


Figure 11-5: **S-R Latch**

(a) is the cross-coupled form of the S-R latch circuit
(b) is the gate symbol for the S-R latch

When S = R = 1, the latch oscillates. S = R = 1 is therefore not allowed as an input.

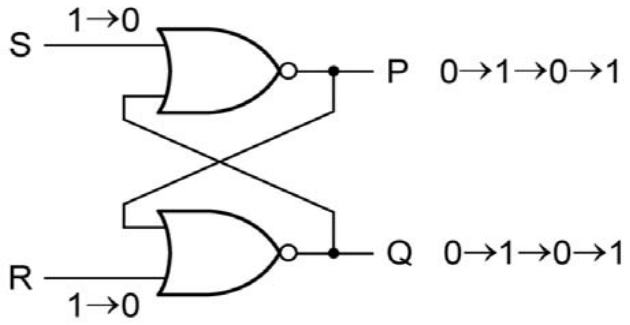


Figure 11-6: **Improper S-R Latch Operation**

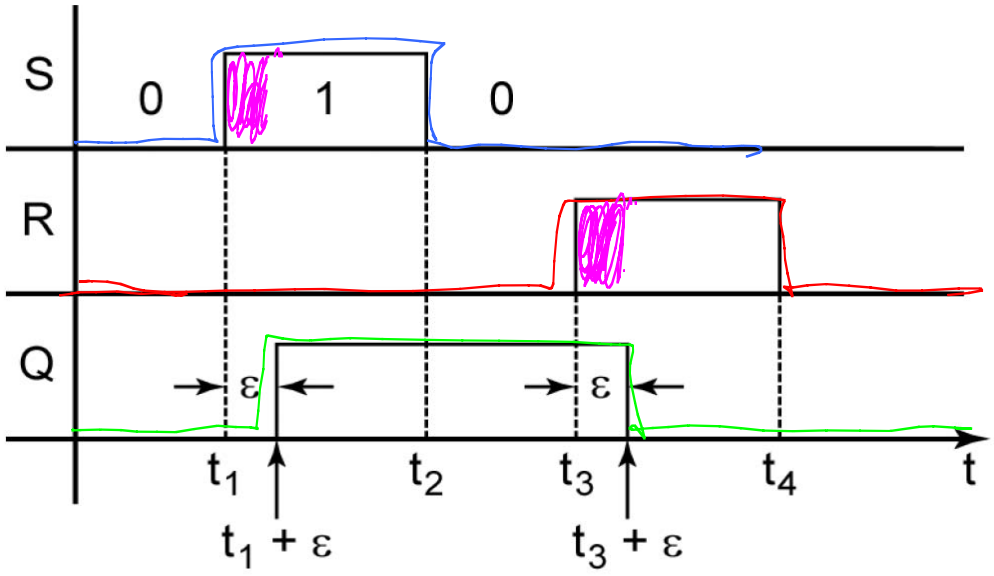


Figure 11-7: **Timing Diagram for S-R Latch**

current state

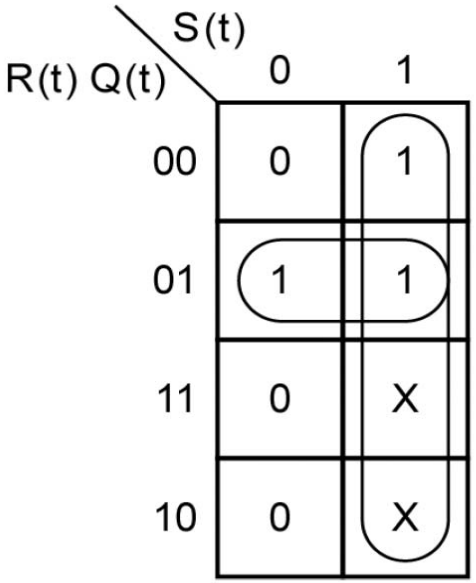
next state

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\epsilon)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	–
1	1	1	–

from 11-3(a) to 11-3(b)

inputs not allowed

Table 11-1. S-R Latch Operation



$Q(t + \varepsilon) = S(t) + R'(t)\, Q(t)$

Figure 11-8: **Map for $Q(t + \varepsilon)$**

$Q^+ = S + R'Q \qquad (SR = 0)$

next state — current state

$S = 1 = R$ is not allowed

characteristic equation or next-state equation of the S–R latch

We will see several other latches & flip-flops and their characteristic equations!