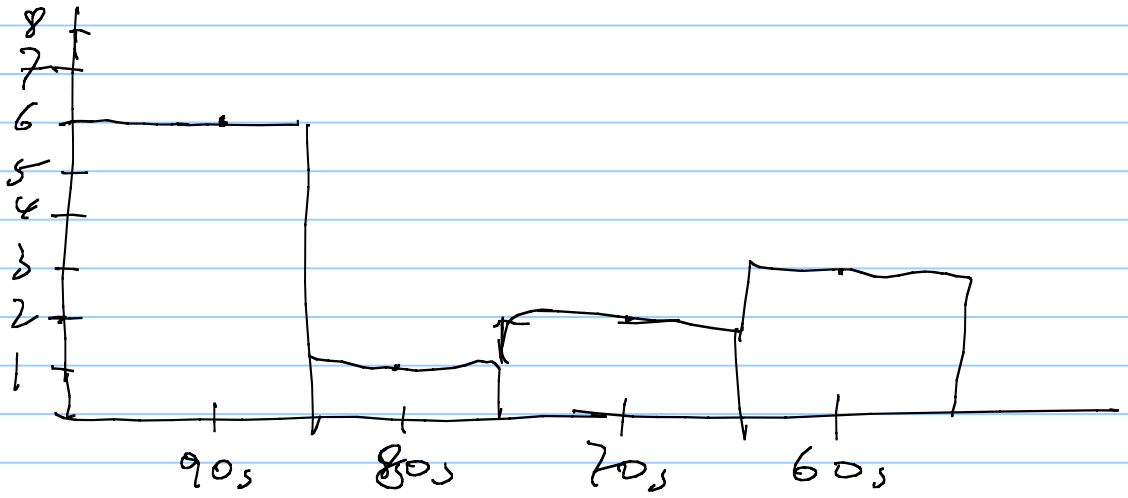
Note Title 3/23/2009

HW 4 results:

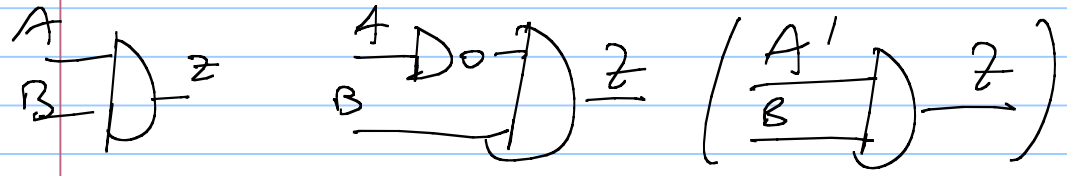


Please review solutions from the notes for last Friday's class (2008-03-25)

Circuit 2 is based on Chs. 5+7: you will design a circuit using K-maps (Karnaugh maps) and implement it with NAND gates. Due in one week — March 30.

Chapter 7: Multi-level gate Circuit, NAND & NOR Gate

We do not count inverters at the inputs of a circuit



have the same number of levels, namely one

The number of levels of a circuit is the maximum number of gates between an input and the output of that circuit, with the proviso that inverters at the inputs of a circuit are not counted.

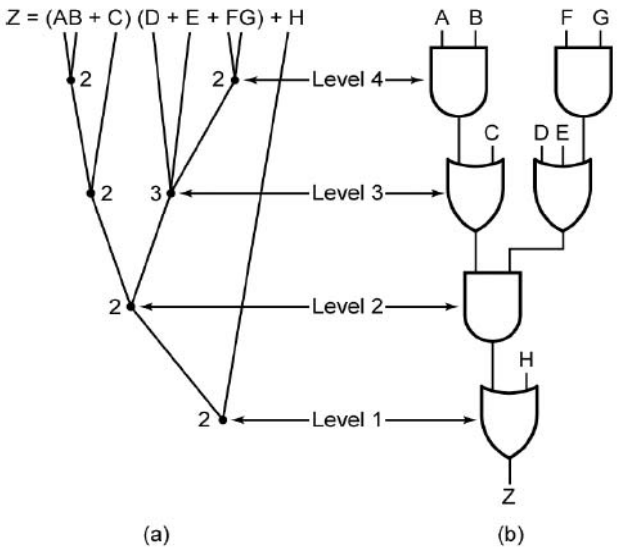


Figure 7-1: **Four-Level Realization of Z**

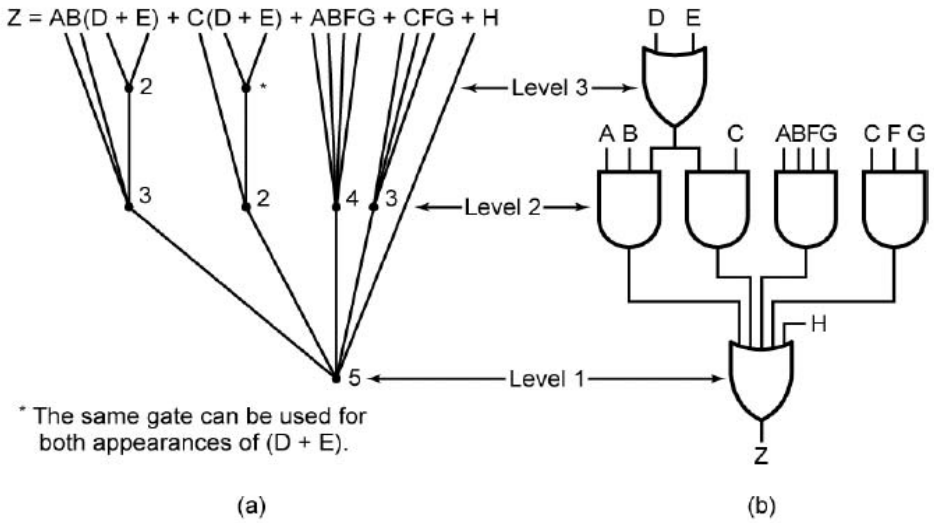


Figure 7-2: **Three-Level Realization of Z**

4 levels, 6 gates, 13 gate inputs

3 levels, 6 gates, 19 gate inputs

$$Z = (AB + C)(D + E + FG) + H = (AB + C)[(D + E) + FG] + H =$$

$$= AB(D + E) + C(D + E) + (AB + C)FG + H =$$

$$= AB(D + E) + C(D + E) + ABFG + CFG + H$$

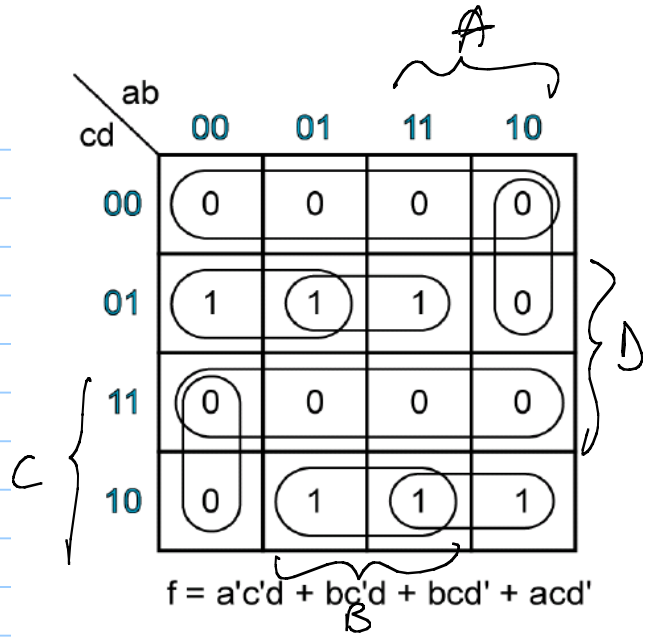
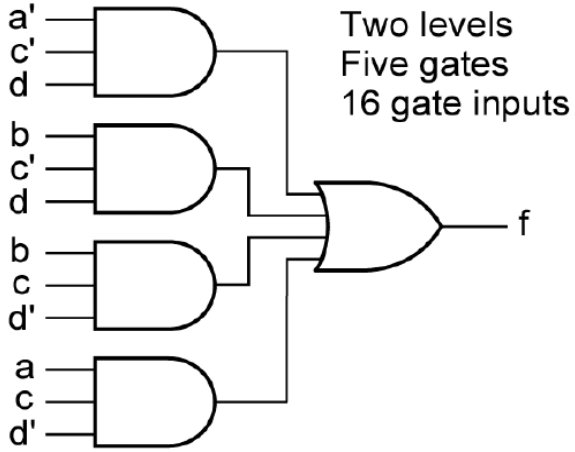


Figure 7-3

$f(a,b,c,d) = \sum m(1,5,6,10,13,14)$

$f = A'C'D + BC'D + ACD' + BCD'$



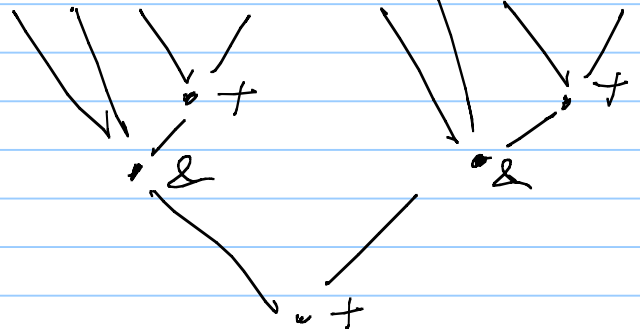
minimal SOP realization

AND–OR

Figure 7-4

Factor f: $f = c'a(a'+b) + ca'(a+b)$

OR-AND-OR circuit



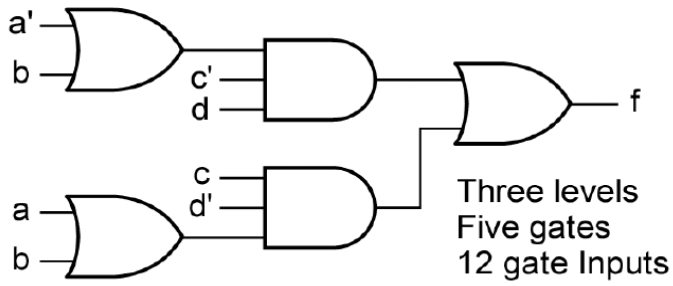


Figure 7-5

$f' = c'd' + ab'c' + cd + a'b'c$ POS

$f = (f')' = (c+d)(a'+b+c)(c'+d')(a+b+c')$

OR-AND circuit

$(x+y)(x+z) = x + yz$

$f = [c+d(a'+b)][c'+d'(a+b)] =$

$= (c + a'd + bd)(c' + ad' + bd')$

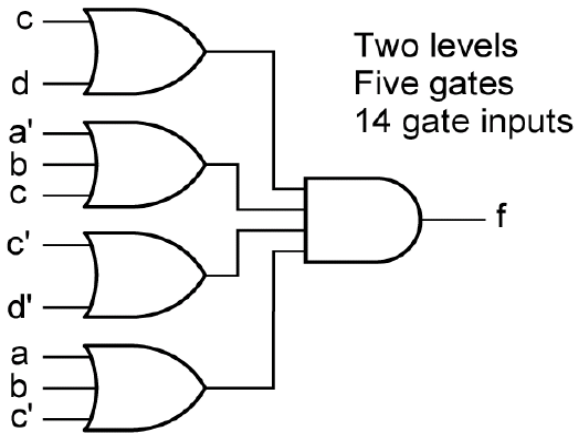


Figure 7-6

OR-AND

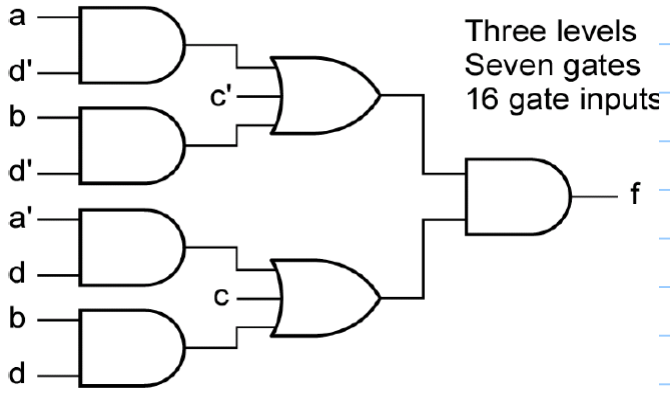
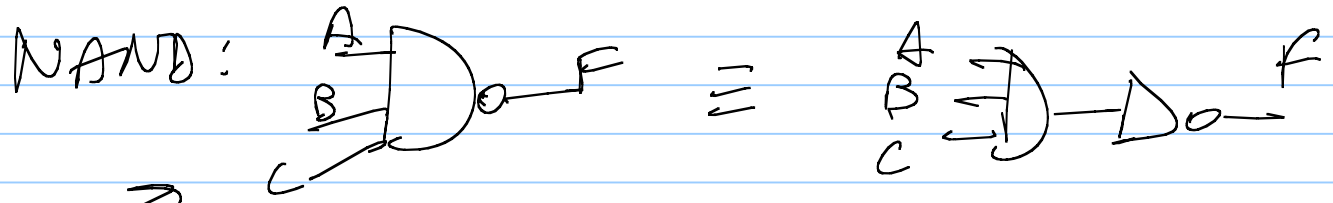
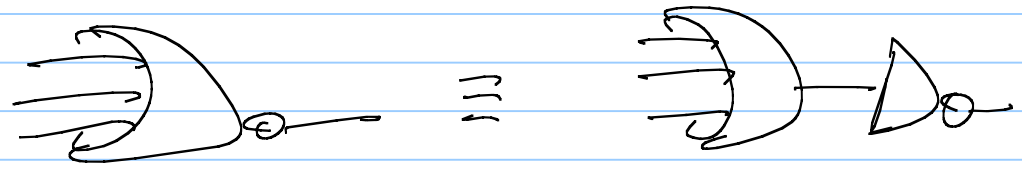


Figure 7-7

AND-OR-AND

NAND: 

AND-NOT gate, but it is customarily called NAND gate
of 3 input



NOR

OR-NOT gate, customarily called NOR.