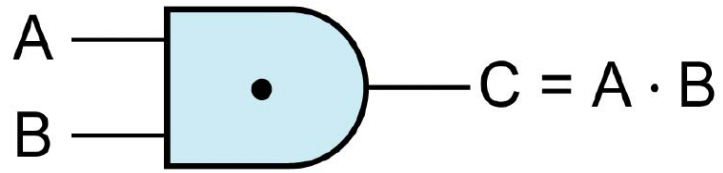
Note Title 2/5/2009

HW 2 correction ✓

Figures are from the text

A truth table (a.k.a. combination table): The truth table for AND ("logic product")

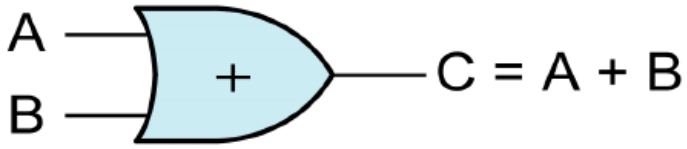
| A B | C = A • B |
|---|---|
| 0 0 | 0 |
| 0 1 | 0 |
| 1 0 | 0 |
| 1 1 | 1 |




(conjunction)

| A B | C = A + B |
|---|---|
| 0 0 | 0 |
| 0 1 | 1 |
| 1 0 | 1 |
| 1 1 | 1 |

The truth table for OR (∨, +)
("logical sum")



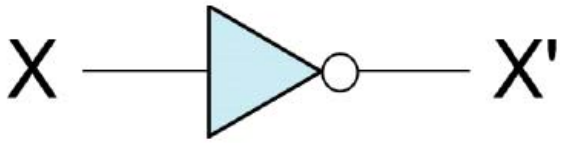

The OR gate (disjunction)

X' = 1 if X = 0
X' = 0 if X = 1

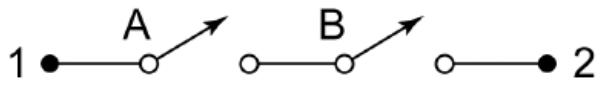
| X | X' |
|---|---|
| 0 | 1 |
| 1 | 0 |

The truth table for negation

$X'$ or $\overline{X}$ or $\sim X$ or $\neg X$ or not X or not(X) or (NOT X)




The inverter circuit element




T = 0 open circuit between terminals 1 and 2

T = 1 closed circuit between terminals 1 and 2

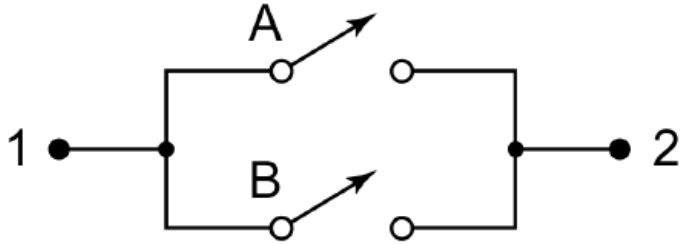
T = AB

T is the transmission between terminals 1 and 2

T=0 ≡ no transmission between 1 & 2

T=1 ≡ transmission between 1 & 2.

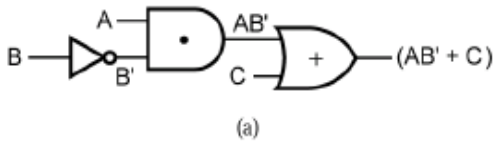
(A series circuit: a series of two switches)




T = A+B

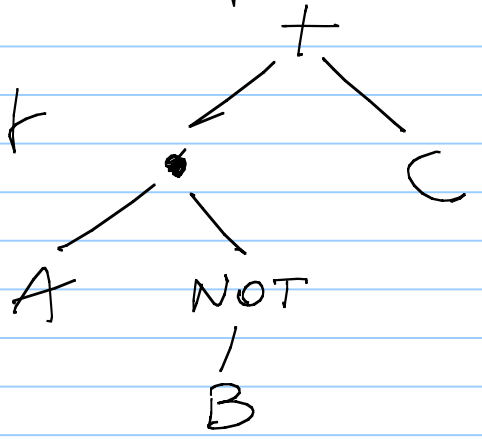
A parallel circuit.

Transmission between 1 and 2 is a faithful model of A+B.



(a)

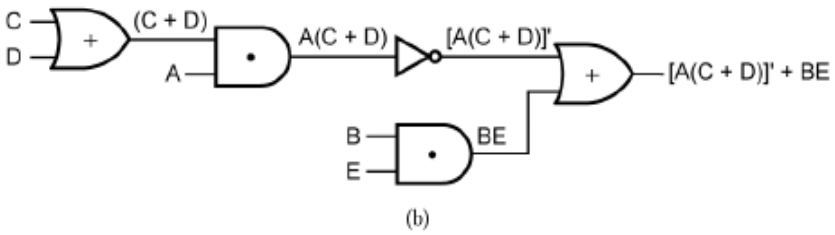
A tree representation of this circuit



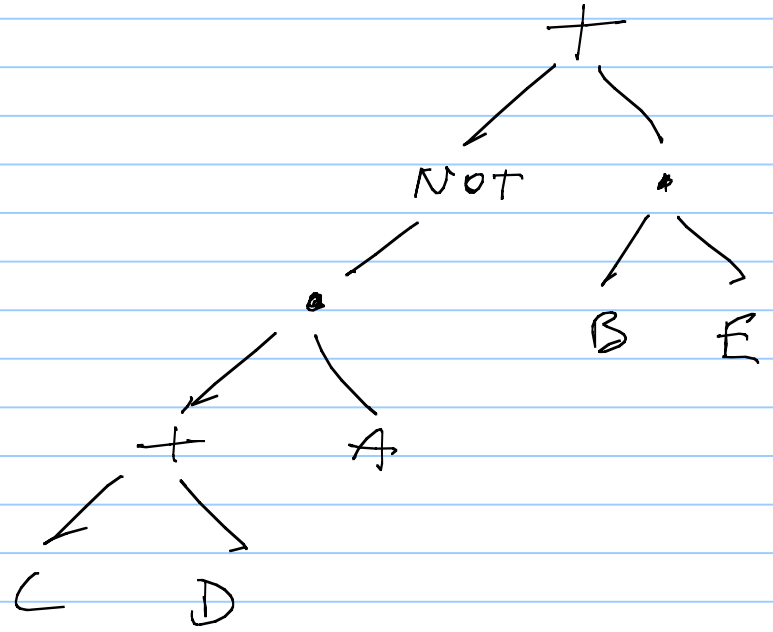

$((A \cdot B') + C)$

We omit parentheses by associating AND more tightly than OR, and NOT more tightly than AND

So $((A \cdot B') + C) = A \cdot B' + C = (\text{omit } \cdot) = AB' + C$

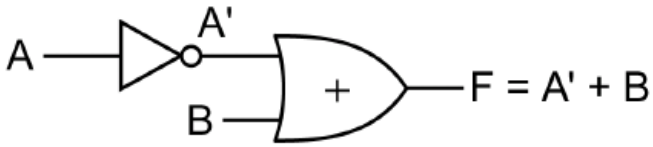



(b)




$$\left[\left(\text{NOT}\left((C+D)\cdot A\right) + (B\cdot E)\right)\right.$$

$$= \left(A(C+D)\right)' + BE$$




| A B | A′ | F = A′ + B |
|---|---|---|
| 0 0 | 1 | 1 |
| 0 1 | 1 | 1 |
| 1 0 | 0 | 0 |
| 1 1 | 0 | 1 |

(b)

*Figure 2-2:* **2-Input Circuit**